

MK0520 LDMOS TRANSISTOR

Document Number: MK0520
Product Datasheet V3.0

200W, 28V High Power RF LDMOS FETs

Description

The MK0520 is a 200-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 1 GHz. It can be used in Class AB/B and Class C for all typical modulation formats.

• Typical Performance (On Innogration fixture with device soldered):

$V_{DD} = 28$ Volts, $I_{DQ} = 1000$ mA, CW.

Frequency	Gp (dB)	P_{-1dB} (W)	$\eta_D@P_{-1}$ (%)
1000 MHz	17	200	60

• Typical Performance (On Innogration fixture with device soldered):

$V_{DD} = 28$ Volts, $I_{DQ} = 850$ mA, CW.

Frequency	Gp (dB)	P_{-1dB} (W)	$\eta_D@P_{-1}$ (%)
10 MHz	19.8	80	45.1
20 MHz	20.2	114	55.6
30 MHz	20.0	127	58.8
60 MHz	20.5	157	65.1
100 MHz	20.2	141	50.4
200 MHz	20.3	185	58.1
300 MHz	20.3	186	55.4
400 MHz	19.7	180	58.9
500 MHz	18.6	135	51.5
600 MHz	17.2	90	55.3

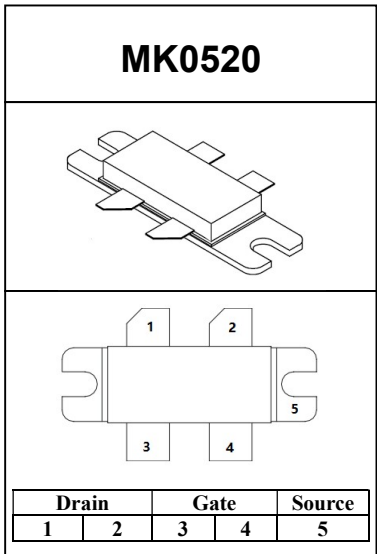


Figure 1. Pin Connection

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+40	Vdc

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Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _c = 85°C, T _j = 200°C, DC test	R _{θJC}	0.35	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics (per half section)

Drain-Source Voltage V _{GS} = 0, I _{DS} = 1.0mA	V _{(BR)DSS}	95	98		V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 75V, V _{GS} = 0 V)	I _{DSS}	—	—	1	μA
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 V, V _{GS} = 0 V)	I _{DSS}	—	—	1	μA
Gate--Source Leakage Current (V _{GS} = 10 V, V _{DS} = 0 V)	I _{GSS}	—	—	1	μA
Gate Threshold Voltage (V _{DS} = 28V, I _D = 600 μA)	V _{GS(th)}	—	2.19	—	V
Gate Quiescent Voltage (V _{DD} = 28 V, I _D = 700 mA, Measured in Functional Test)	V _{GS(Q)}	—	3.05	—	V
Common Source Input Capacitance (V _{GS} = 0V, V _{DS} = 28 V, f = 1 MHz)	C _{ISS}		106		pF
Common Source Output Capacitance (V _{GS} = 0V, V _{DS} = 28 V, f = 1 MHz)	C _{OSS}		40		pF
Common Source Feedback Capacitance (V _{GS} = 0V, V _{DS} = 28 V, f = 1 MHz)	C _{RSS}		1.6		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1000 mA, f = 1000 MHz, CW Signal Measurements.

Power Gain	G _p	—	17	—	dB
Drain Efficiency@P1dB	η _D	—	60	—	%
1 dB Compression Point	P _{-1dB}	—	200	—	W
Input Return Loss	IRL	—	-7	—	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 1000 mA, f = 1000 MHz

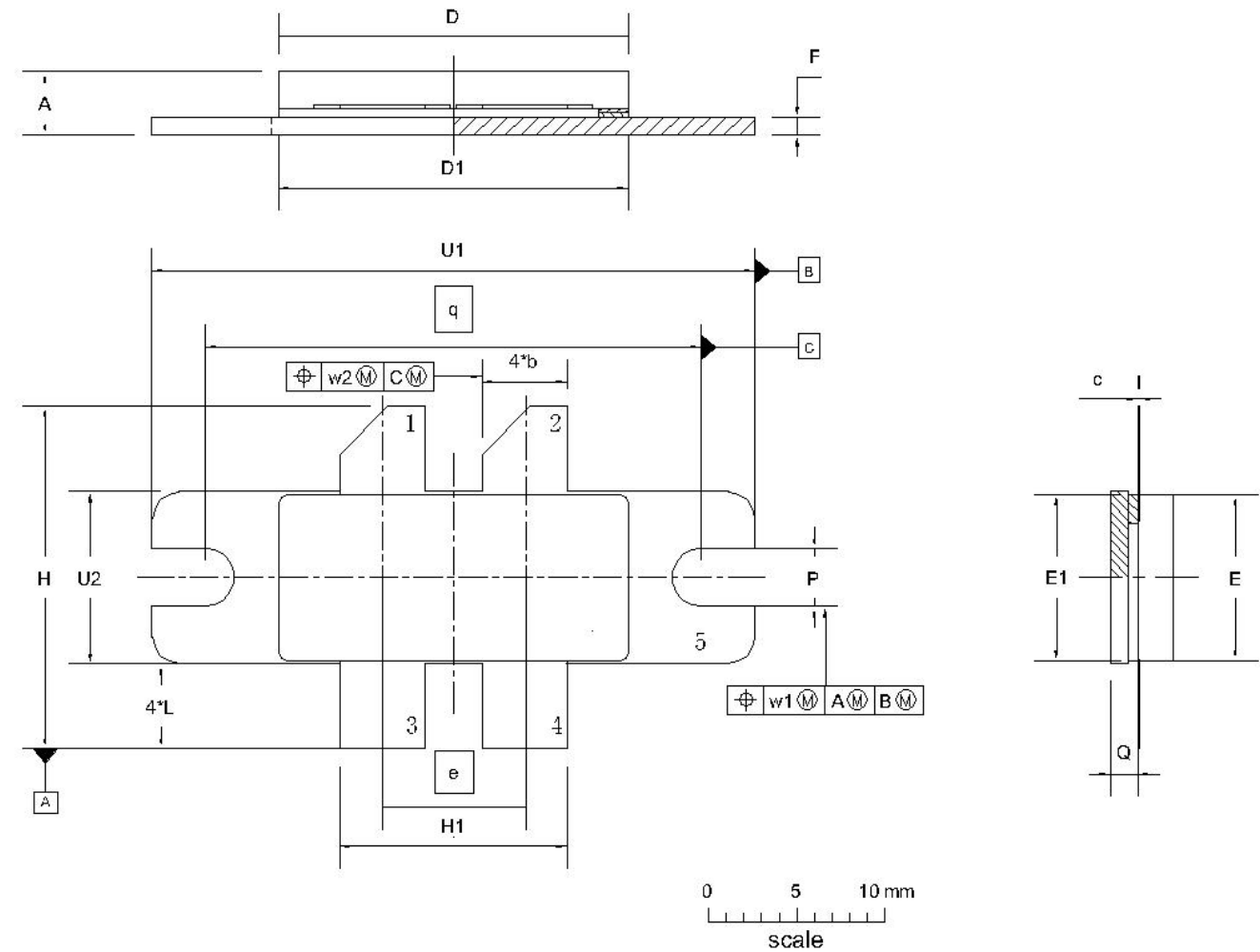
VSWR 20:1 at 200W pulse CW Output Power	No Device Degradation
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Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	p	Q	q	U ₁	U ₂	W ₁	W ₂
mm	4.72	3.94	0.15	20.02	19.96	8.89	9.50	9.53	1.14	19.94	12.83	5.33	3.38	1.70	27.94	34.16	9.91	0.25	0.51
	3.43	3.68	0.08	19.61	19.66		9.30	9.25	0.89	18.92	12.57	4.32	3.12	1.45		33.91	9.65		
inches	0.186	0.155	0.006	0.788	0.786	0.35	0.374	0.375	0.045	0.785	0.505	0.210	0.133	0.067	1.100	1.345	0.390	0.01	0.02
	0.135	0.145	0.003	0.772	0.774		0.366	0.364	0.035	0.745	0.495	0.170	0.123	0.057		1.335	0.380		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4E					03/12/2013

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2015/4/16	Rev 1.0	Preliminary Datasheet
2016/8/8	Rev 2.0	Preliminary Datasheet
2017/2/22	Rev 3.0	Product Datasheet

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